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PATENT COOPERATION TREATY

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From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
LESTER J. VINCENT
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RECEIVED DEC 16 2006 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	
Applicant's or agent's file reference 006450.P003PCT	IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US04/41119	08 December 2004 (08.12.2004)	08 December 2003 (08.12.2003)

Applicant

CADENCE DESIGN SYSTEMS, INC.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. REMINDER

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Jack Chiang Telephone No. (571) 272-2800

PATENT COOPERATION TREATY

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PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 006450.P003PCT	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US04/41119	International filing date *(day/month/year)* 08 December 2004 (08.12.2004)	Priority date *(day/month/year)* 08 December 2003 (08.12.2003)

International Patent Classification (IPC) or national classification and IPC

IPC: G06F 17/50(2006.01) G06F 17/50(2006.01)
USPC: 716/3

Applicant

CADENCE DESIGN SYSTEMS, INC.

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 10 sheets, including this cover sheet.

☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of — sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
- IV ☒ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
07 July 2005 (07.07.2005)	20 September 2006 (20.09.2006)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Jack Chiang Telephone No. (571) 272-2800

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US04/41119

I. Basis of the report

1. With regard to the elements of the international application:*

☒ the international application as originally filed.

☒ the description:
pages 1-28 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages 29-34, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-7, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US04/41119

IV. Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees the applicant has:

☐ restricted the claims.

☐ paid additional fees.

☐ paid additional fees under protest.

☒ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention is accordance with Rules 13.1, 13.2 and 13.3 is

☐ complied with.

☒ not complied with for the following reasons:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claim(s) 1-14 and 21-30, drawn to a design method for transforming sequential logic designs into equivalent combinational logic..

Group II, claim(s) 15-20 and 31-34, drawn to a back tracking design method for transforming sequential logic designs into equivalent combinational logic.

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention referred to a design method comprising simulating each stage of a clocking sequence to produce and record simulation values while the special technical features of the Group II invention is a backtracking method comprising determining whether or not a time T is negative and producing a block B tied to an unknown logic. Because the special feature of the Group I invention is not present in the Group II claims and because the special feature of the Group II invention is not present in the Group I claims, unity of invention is lacking.

4. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

☐ all parts.

☒ the parts relating to claims Nos. 1-14 and 21-30

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US04/41119

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	9, 25	YES
	Claims	1-8, 10-15, 21-24, 26-30	NO
Inventive Step (IS)	Claims	9, 25	YES
	Claims	1-8, 10-15, 21-24, 26-30	NO
Industrial Applicability (IA)	Claims	1-14, 21-30	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

V. 2. Citations and Explanations:
Claims 1-8, 10-15, 21-24 and 26-30 lack novelty under PCT Article 33(2) as being anticipated by Girald et al., "A Trace-Based Method for Delay Fault Diagnosis in Synchronous Sequential Circuits," IEEE, 1995, pages 526-532.

As to claims 1, 5 and 21, Girard et al. teach a trace-based method for delay fault diagnosis in synchronous sequential circuits (see pages 526-532). The method comprises forming modeling for sequential circuits, where a sequential circuit can be modeled as composed of a combinational part and a memory part. Fig. 1 show iterative array model for a sequential circuit that is formed by an array of combinational circuits. The method also comprises simulating each stage of clocking sequence (slow clock and fast clock) on the sequential logic design as described above to produce simulation values and saving the simulation values (page 528, under section 5, Girard et al. teach the signal values on each line in the activation and propagation phases are recorded in order to be used later by the critical path tracing process. Again, Girard et al. teach starting page 528 under section 5. The trace-based method to provide an equivalent combinational logic representation of the sequential logic design.

As to claims 2 and 22, Girard et al. teach for each time "T" (time frame) of the clocking sequence, each block being measured at the time T is traced (see Fig. 1-4, see section 5. The trace-based method).

As to claims 3 and 23, Girard et al. teach circuit modeling for sequential circuits that is composed as of a combinational pare and a memory part. The boundaries of the combinational logic consist of primary inputs (data input), primary outputs (data output) and flip-flops (FF's) (Fig. 1). Section 5 describes a trace-based method for sequential circuits including a multi-values simulations and critical path tracing, where a primary output is traced backed (see section 5.1-5.2).

As to claims 4 and 24, Girard et al. teach multi-valued simulations for sequential circuits (starting page 529). Since the sequential circuits includes flip-flops or memory part (scan cells), simulating the sequential circuits as taught by Girard et al. include simulating scan operations by placing the sequential circuit in its scan state (see section 3, page 528).

As to claim 6, Girard et al. teach at the end of initialization sequence, all flip-flops (scan cells) are set into states required by the fault activation vector. Next, the fault is activated by applying Vi and using a fast clock. Concepts of testing for delay faults in combinational or scan-based circuits are applicable in this phase (see section 3, page 528). The scan-based circuits testing require setting scan control inputs to their scan-enable values.

As to claims 7-8, Girard et al. teach simulating sequential circuits by modeling the circuit as combinational circuit part and memory part to provide equivalent combinational circuit (Fig. 1). The simulation is performed by slow clock and fast clock, therefore in order to perform with fast clock, the rest of clocks (slow clock) must be turned off.

As to claim 10, Girard et al. teach a method for diagnosing gate delay faults in synchronous sequential circuits based on a path tracing algorithm appropriate sequential circuits to produce a combinational circuit equivalent (see section 6).

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US04/41119

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

As to claims 11-12 and 27-28, Girard et al. teach modeling sequential circuits as a combination part and memory part (partitioning the sequential design into smaller pieces) and processed on separate computing device (see section 2).

As to claims 13 and 29, Girard et al. simulating the sequential circuits based on fast clock cycles (sampled clock or chopped clocks) (see section 4).

As to claims 14 and 30, Girard et al. simulating the sequential circuits based on fast clock cycles (chopped clocks) and the signal values on each line in activation and propagation phases are recorded in order to be used later by the critical path tracing process (see page 528, section 5).

As to claim 26, Girard et al. teach the operations are used for automatic test pattern generation (See section 4).

Claims 9 and 25 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest simulating primary input force events by turning off all of the clock inputs to the design.

Claims 1-15 and 21-30 meet the criteria set out in PCT Article 33(4), and thus are useful in industrial applicability because the subject matter claimed can be made or used in industry.

---------- NEW CITATIONS ----------

Girald et al., "A Trace-Based Method for Delay Fault Diagnostis in Synchronous Sequential Circuits," IEEE, 1995, pages 526-532.